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Wafer-Scale Arrays of Nonvolatile Polymer Memories with Microprinted Semiconducting Small Molecule/Polymer Blends

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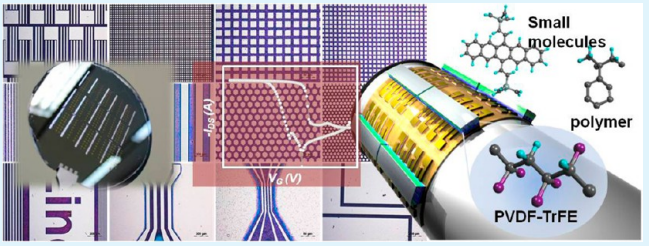
Supporting Information

ABSTRACT: Nonvolatile ferroelectric-gate field-effect transistors (Fe-FETs) memories with solution-processed ferroelectric polymers are of great interest because of their potential for use in low-cost flexible devices. In particular, the development of a process for patterning high-performance semiconducting channel layers with mechanical flexibility is essential not only for proper cell-to-cell isolation but also for arrays of flexible nonvolatile memories. We demonstrate a robust route for printing large-scale micropatterns of solution-processed semiconducting small molecules/insulating polymer blends for high performance arrays of nonvolatile ferroelectric polymer memory. The nonvolatile memory devices are based on top-gate/bottom-contact Fe-FET with ferroelectric polymer insulator and micropatterned semiconducting blend channels. Printed micropatterns of a thin blended semiconducting film were achieved by our selective contact evaporation printing, with which semiconducting small molecules in contact with a micropatterned elastomeric poly(dimethylsiloxane) (PDMS) mold were preferentially evaporated and absorbed into the PDMS mold while insulating polymer remained intact. Well-defined micrometer-scale patterns with various shapes and dimensions were readily developed over a very large area on a 4 in. wafer, allowing for fabrication of large-scale printed arrays of Fe-FETs with highly uniform device performance. We statistically analyzed the memory properties of Fe-FETs, including ON/OFF ratio, operation voltage, retention, and endurance, as a function of the micropattern dimensions of the semiconducting films. Furthermore, roll-up memory arrays were produced by successfully detaching large-area Fe-FETs printed on a flexible substrate with a transient adhesive layer from a hard substrate and subsequently transferring them to a nonplanar surface.



KEYWORDS: *microprinting, nonvolatile memory, selective contact evaporation printing, large-area memory arrays, small molecule and polymer blend micropatterns, roll-up polymer memory*

1. INTRODUCTION

High-performance nonvolatile ferroelectric memories with solution-processed ferroelectric polymers, along with other organic nonvolatile memory technologies (such as resistive[1,2] and flash[3,4] memories), are of great interest because of their low production costs and their potential for use in flexible devices, which are of interest in many emerging mobile applications.[5−9] Poly(vinylidene fluoride) (PVDF) and its copolymers with trifluoroethylene (TrFE) (PVDF-TrFE) are representative ferroelectric polymers in which ferroelectric switching is accompanied by facile rotation of the bistable permanent dipole between the hydrogen and fluorine atoms along the polymer chain upon altering the polarity of an electric field.[10] In particular, ferroelectric-gate field-effect transistors (Fe-FETs)[11,12] with ferroelectric polymer gate insulators have attracted great attention because of their additional benefits of non-destructive memory operation through a semiconducting channel, scalable feature size, and low operating voltages.[5,7] Significant progress in the memory performance of Fe-FETs has been made since their first demonstration[11,12] through the addressing of various scientific and technical issues, including nondestructive readout capability,[5,6,13,14] scalability, flexibility,[14] printability,[15] endurance,[5,16] long data retention,[5,6,14] short program pulse width,[5] large ON/OFF ratio,[5,6,13−15] and multi-level modulation.[17] Furthermore, advances in materials design have also been achieved in electrodes,[5] ferroelectric and insulating layers[6,14] and semiconducting active channel layers.[5,6,13−15,18−22]

However, most of the previous efforts to improve Fe-FETs focused on resolving and improving the issues based on the unit device cell, and only a few works have addressed the fabrication of arrays of memory elements with statistically averaged large-area device performance. In particular, the development of a process for patterning semiconducting channel layers is essential for proper cell-to-cell isolation to reduce parasitic current paths between neighboring devices. Furthermore, the development of micropatterns for high performance organic semiconductors with mechanical flexibility is in high demand for the arrays of flexible nonvolatile memories which ensure a high ON/OFF ratio for the sufficient bistability margin and high charge carrier mobilities for fast switching. The structural integrity of these patterns must be

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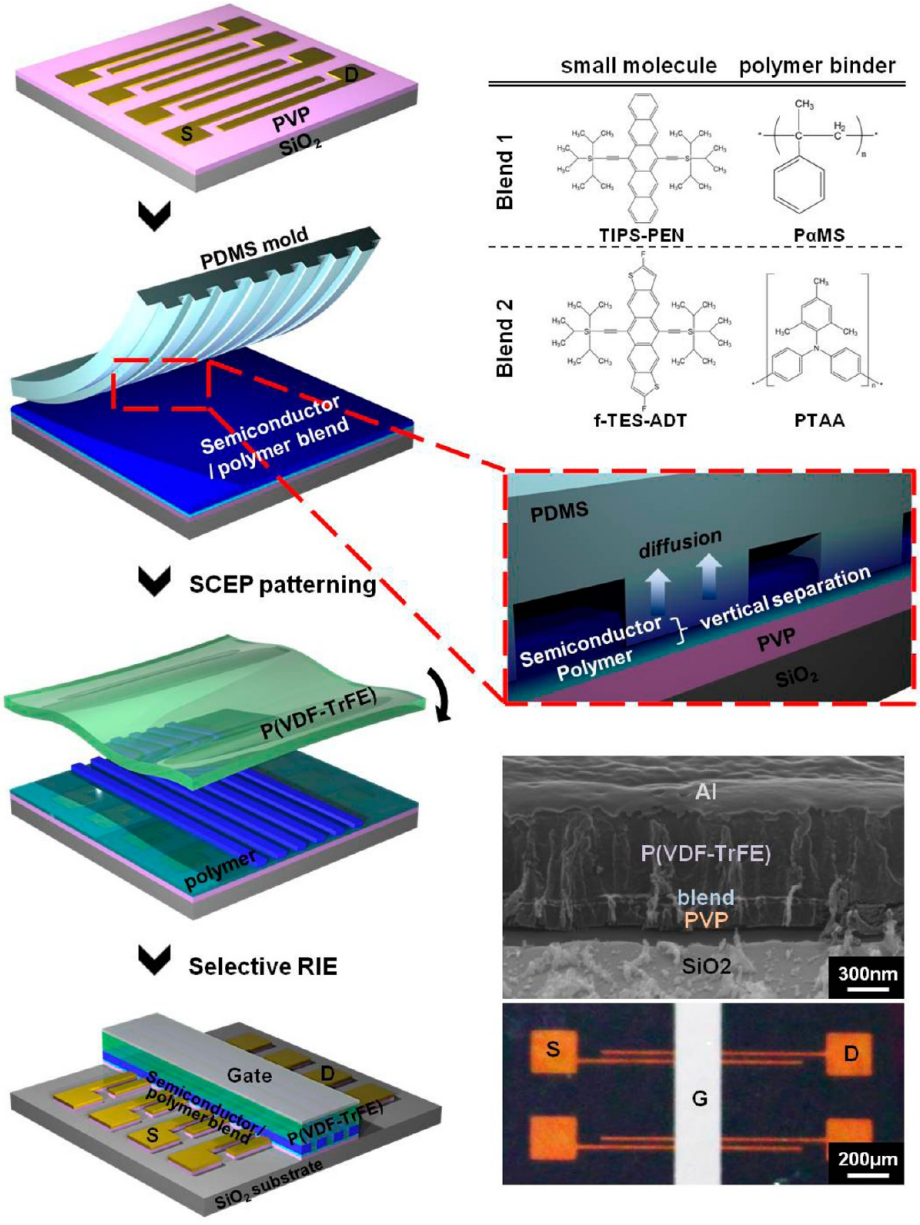

Figure 1. Schematic illustration of the fabrication of large-area printed Fe-FET arrays with micropatterned semiconducting channels of solution-blended small molecule semiconductors and polymer insulator films. Two types of binary blend films, the chemical structures of which are shown on the right-hand side, were prepared by spin-coating on patterned Au S/D electrode arrays. Subsequent SCEP with a topographic PDMS mold placed on the blend film with appropriate heat and pressure allowed for fabrication of a well-defined micropatterned structure on the film by the selective evaporation and diffusion of small molecule semiconductors on the contact regions with the PDMS mold, as shown in the red box. The monolithic transfer of a ferroelectric PVDF-TrFE film on the patterned blend film followed by thermal evaporation of the top-gate Al electrodes produced a top-gate/bottom-contact Fe-FET array with micropatterned semiconducting channels. The SEM micrograph (top) and a photographic image (bottom) show a cross-sectional view of a Fe-FET and a plane view of two Fe-FETs sharing a common top gate, respectively.

also maintained during device fabrication. For instance, a patterned semiconductor should not be damaged upon deposition of a solution-processed ferroelectric insulator on the pattern in the top-gate Fe-FET architecture, as this provides more reliable memory operation due to auto-encapsulation of air-sensitive organic semiconductors by the overlaid gate insulator and electrode.[23]

Small molecule semiconductor and insulating polymer blend layers have been extensively investigated as channel layers for organic field effect transistors (OTFTs) due to their high semiconducting properties (arising from small molecule semiconductors) as well as the good film formation and mechanical flexibility of the amorphous binder polymers.[24−36] Previous studies of OTFTs[31,37] have clearly shown that these blended channel layers are also beneficial for high performance and reliable large-area arrays of Fe-FETs when appropriately micropatterned with solution-processed ferroelectric polymer insulators. In fact, for nonvolatile ferroelectric memories with small molecule semiconducting channels, vacuum-deposited pentacene has been dominantly used and only a few works demonstrated arrays of Fe-FETs.[19,20,38−40] The patterns of pentacene channels were, therefore, developed by thermal deposition with a shadow mask, making it difficult to fabricate large area arrays of memories. Although the various non-

destructive patterning methods for crystalline small molecule semiconductors have been developed such as transfer printing,[41,43] inkjet printing,[37] contact evaporation printing,[42] and micromolding in capillaries,[44] only a few can be applied for fabrication of micropatterns of thin and uniform semiconducting blend films for flexible organic electronic devices including OTFTs and Fe-FETs without complicated additional processes such as etching and lift-off.

In this work, we present large-area printed arrays of nonvolatile top gate-bottom contact Fe-FET memories with solution-processed micropatterns of semiconducting small molecule/insulating polymer blends. Two pivotal processes were employed: (1) large-area printing of a semiconducting blend film by Selective Contact Evaporation Printing (SCEP)[42] and (2) monolithic transfer of a thin ferroelectric polymer film. The process employed two types of organic semiconducting small molecules/amorphous polymer blend films of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-PEN)/ poly-(alpha methylstyrene) (PαMS) and 2,8-difluoro-5,11-bis-(triethylsilylethynyl) anthradithiophene (diF-TES-ADT)/Poly-[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA). SCEP allowed for the successful fabrication of well-defined micrometer-scale patterns with various shapes and dimensions, which could be readily fabricated over a very large area, i.e., a 4 in. wafer. Arrays of Fe-FETs in combination with monolithic transfer of a spin-coated ferroelectric polymer film on the micropattern exhibited highly uniform and reliable device performance. Furthermore, utilization of a mechanically flexible substrate with transient adhesive layer allowed for the fabrication of roll-up memory arrays on a curved surface.

2. EXPERIMENTAL SECTION

Materials. TIPS-PEN (99.9% purity) was purchased from Sigma-Aldrich, Korea. TIPS-PEN (3 wt %) and poly(alpha-methylstyrene) (M_w = 100 kDa) (Sigma-Aldrich Korea) were dissolved in a tetralin solvent at a 50:50 blending ratio. DiF-TES-ADT (99% purity, Sigma-Aldrich Korea) and PTAA (average Mn 7-10 k, Aldrich) were dissolved in a tetralin solvent at 4 wt % concentration with a 50:50 ratio of components. A ferroelectric P(VDF-TrFE) copolymer 75:25 of PVDF:TrFE used in this work was kindly supplied by MSI Sensor, PA, and has melting (T_m) and Curie (T_c) temperatures of 150°C and 80°C, respectively. A 10 wt % PVP solution in propylene glycol monomethyl ether acetate (PGMEA) with poly(melamine-co-formaldehyde) was used as a cross-linking agent.

Selective Contact Evaporation Printing (SCEP). A variety of elastomeric PDMS molds were fabricated by curing PDMS precursor (Sylgard 184, Dow Corning Corp) on a pre-patterned Si master. We used a mixture of PDMS precursor and curing agent (10:1 by weight) that had been degassed under vacuum. The pre-patterned photoresist masters were prepared by standard photolithography, and the surface of the master was fluorinated before casting the PDMS precursor on the master. After the PDMS precursor was cured at 60°C for 6 h using a vacuum oven, the mold was separated from the master. PDMS molds are available with one-dimensional periodic lines having several sizes ranging from 2 to 100 μm. A topographically pre-patterned PDMS mold was placed in conformal contact on the semiconductor/polymer blend film. When conformal contact of PDMS was initiated with appropriate pressure (3 kPa), small molecules were heated to 100 °C for 1 h.

Fabrication of Fe-FET Memory Array. Fabrication of a ferroelectric-gate field-effect transistor (Fe-FET) memory with patterned active channels starts with the formation of a 200 nm thick PVP film on a SiO_2 substrate (altered with the polyimide substrates for the flexible device) in order to achieve good film formation using small molecules and polymer blends. Subsequently, the films were cross-linked by curing at 200 °C for 30 min. The 30 nm thick Au source and drain arrays were thermally deposited on cross-linked PVP thin films using a shadow mask under a pressure of 1×10^{-6} mbar and rate of 0.1 nm/s. Semiconductor and polymer blend thin films were formed by spin-coating at 500 rpm for 10 s and then at 2000 rpm for 20 s. All films were annealed at 100 °C for 5 min to remove excess solvent. The small-molecule thin film was patterned with 20 μm and 50 μm line-shaped hole transport active channels connected between the source and drain electrodes by SCEP. A spin-coated PVDF-TrFE film was floated from a solid substrate onto the water surface, then transferred onto the micropatterned blend film to prevent possible damage of the active channel layer by the PVDF-TrFE solution. After short thermal annealing at 80°C to remove residual water molecules at the interface between the blend layer and PVDF-TrFE film, the 60 nm thick top gate Al electrodes were deposited by a thermal evaporation system with a shadow mask. Selective O_2 plasma (100 W for 200 s, 1×10^{-3} Torr, 40 sccm) generated by RIE (Femto VITA-4E) was further treated on the device to make the Au source and drain electrodes accessible to the contact probe tips. Al top gate electrode arrays were used as a blocking mask against RIE, allowing for the fabrication of top-gate/bottom-contact Fe-FET memories with source and drain electrodes open to the air, as illustrated in the schematic in Figure 1. The electrical properties of the devices were recorded using a semiconductor system (E5270B, Agilent Technologies). All measurements were done under ambient conditions.

Microstructure Characterization. Scanning electron microscope (SEM) images were obtained with a JEOL JSM-600F field-emission gun electron microscope and a 10 nm thick Pt layer was evaporated on a sample for contrast improvement. Atomic force microscopy (AFM) was performed in height contrast using a Digital Instruments NanoScope 3100 microscope. Optical microscopy (OM) was used to visualize the Fe-FET devices and the patterned blend thin film with an Olympus BX 51M. In particular, a birefringent image of a patterned TIPS-PEN and diF-TES-ADT was obtained under crossed polarizers. Grazing-incidence X-ray diffraction (GIXD) was performed on the 9A beamline at the Pohang Accelerator Laboratory in Korea. The measurements were performed with monochromated X-rays (λ = 0.1381 nm) having grazing incidence angles ranging from 0.09 to 0.15, and the scattered intensity was recorded using a SCX:4300-165/2 CCD detector (Princeton Instruments). The crystalline structure of the semiconductor pattern was characterized by X-ray powder diffraction with monochromatic Cu Kα (λ = 0.154 nm), and selected area electron diffraction (SAED) was performed using a transmission electron microscope (TEM: JEOL JEM-2100F) operated at 200 kV.

3. RESULTS AND DISCUSSION

Fabrication of large-area printed Fe-FETs is schematically illustrated in Figure 1. The thin PVP layer allowed for good formation of a thin small molecule/insulating polymer blend film with a 1:1 composition prepared by spin-coating the blend solution in 1,2,3,4-tetrahydronaphthalene (tetralin) on the patterned source and drain electrodes. Two pairs of binary blends were employed in this work: TIPS-PEN:PαMS and diF-TES-ADT:PTAA. Subsequently, SCEP was performed on the semiconducting small molecule/insulating polymer blend film of approximately 50 nm in thickness as depicted in Figure 1. In the SCEP process, semiconducting small molecules in contact with a micro-patterned elastomeric poly(dimethylsiloxane) (PDMS) mold were preferentially evaporated and absorbed into the PDMS mold while the insulating polymer was left intact, as shown in the red box in Figure 1, allowing for the fabrication of large-area printed semiconducting patterns on a flat insulating polymer. Highly uniform micro-patterns of thin semiconducting small molecule films were readily fabricated after the conformal contact of a PDMS mold on a blend film with appropriate pressure at 100°C for 1 h. These micro-patterns were similar to those of single crystalline semi-

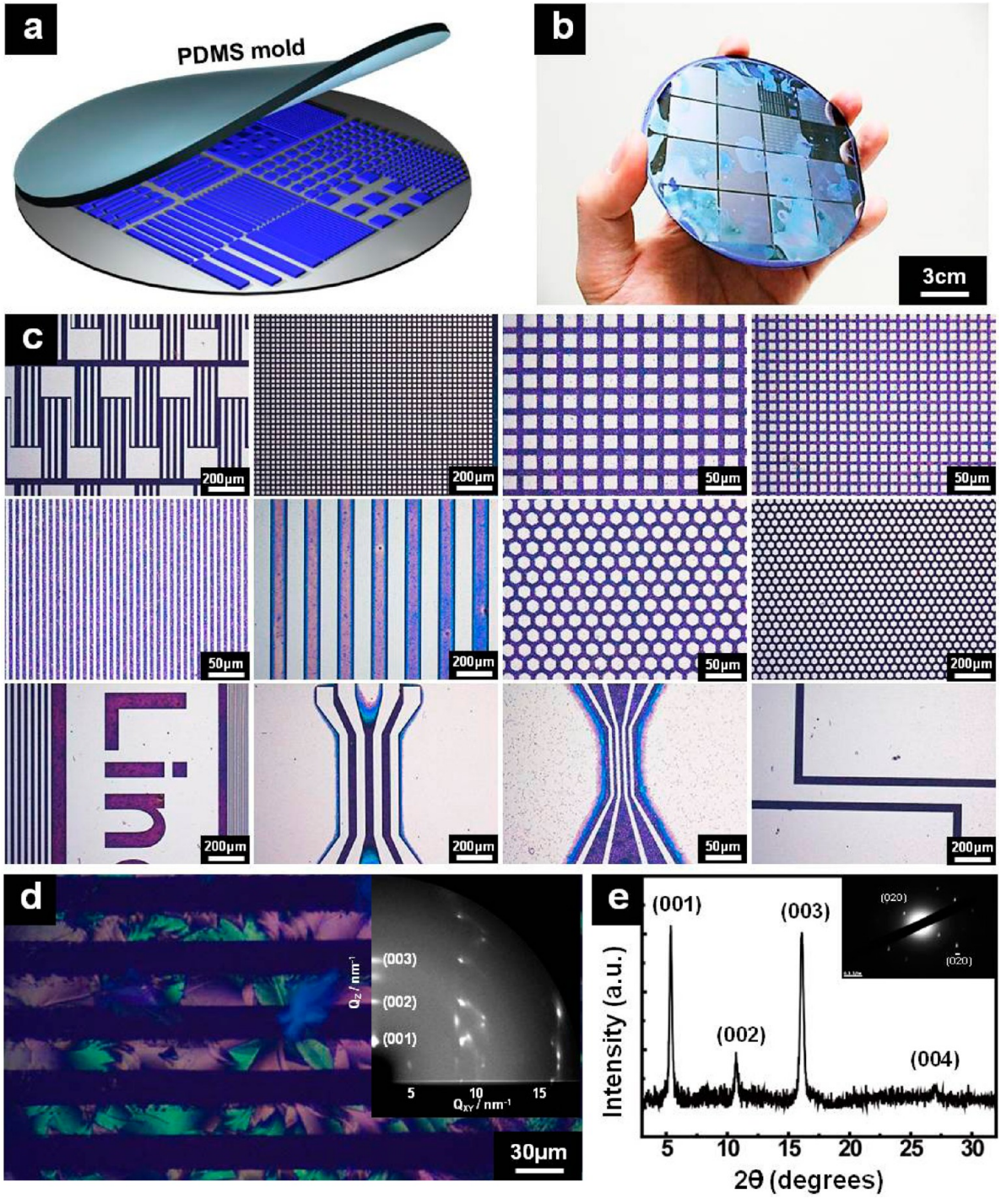

Figure 2. (a) Schematic of micropatterning by SCEP with a 4-inch wafer PDMS mold. (b) Photograph of the wafer-scale micropatterns of thin TIPS-PEN:PαMS film. (c) OM images of different parts of the wafer scale micropatterns with microstructures of various shapes and dimensions, including periodic hexagons, squares, lines, micrometer size letters, and other geometric figures. (d) OM image of the micropatterned periodic lines on the thin TIPS-PEN:PαMS film visualized under crossed polarizers. A 2D-GIXD image of the periodic pattern with single crystalline reflections is shown in the inset of d. (e) Out-of-plane XRD diffraction pattern of the periodic TIPS-PEN:PαMS line pattern. A SAED pattern observed using TEM is also shown in the inset of e.

conductors, as described in our previous report.[42] However, the blended film micropatterning in the current work covers a very large area and gives uniform device performance, whereas the patterning of single-crystalline semiconductors in our previous work was conducted over a limited area and was dependent on the size of the initial single crystals.[42]

Possible damage to the blended semiconductor layer by subsequent spin-coating of a thin ferroelectric PVDF-TrFE film was avoided by the use of a monolithic film transfer technique in which a spin-coated PVDF-TrFE film was floated from a solid substrate onto the water surface, followed by transfer onto the micropatterned blend film. After a short thermal annealing at 80°C to remove the residual water molecules at the contact

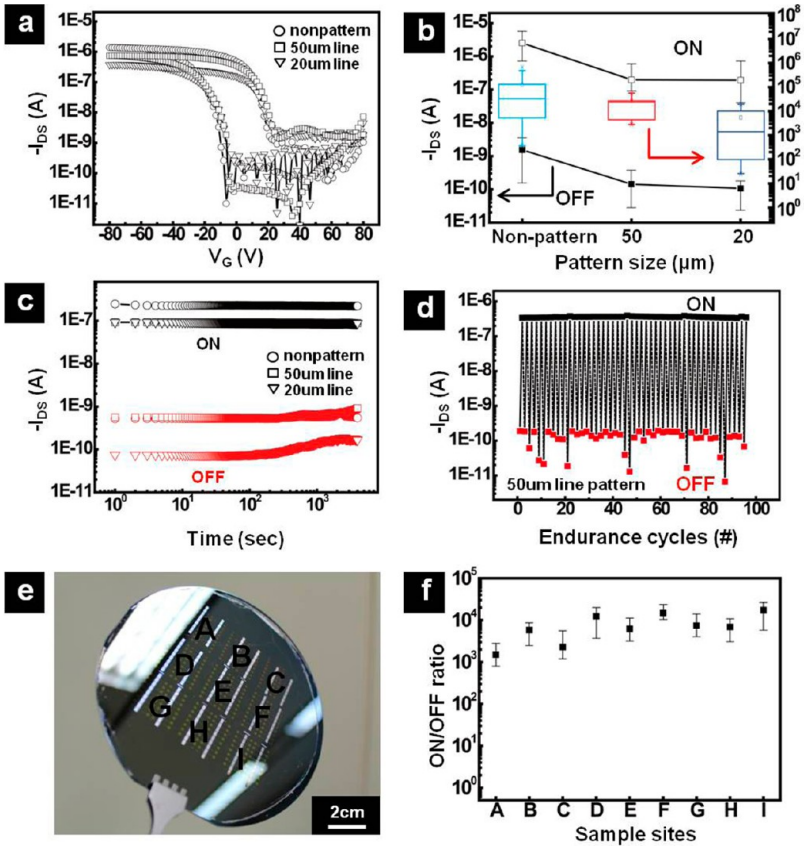

Figure 3. (a) Representative $I_{DS}-V_G$ transfer curves measured at $V_D = -5$ V of the Fe-FETs containing semiconducting channel layers of TIPS-PEN:PαMS of micropatterned 50 μm and 20 μm periodic lines by SCEP. A hysteresis curve of a Fe-FET with a flat TIPS-PEN:PαMS film is also shown for comparison. (b) Statistical distributions of the ON and OFF current levels and the ON/OFF ratios of the hysteresis curves of the Fe-FETs examined in a. (c) Per second time-dependent retention characteristics of the Fe-FETs with micropatterned TIPS-PEN:PαMS channels independently measured with the ON and OFF state drain current . (d) Write/erase endurance cycles of a Fe-FET with 50 μm TIPS-PEN:PαMS lines. (e) Photograph of the arrays of 162 Fe-FET devices with micropatterned semiconducting channels by SCEP fabricated on a 4-inch wafer. (f) Statistical variation of ON/OFF ratios of hysteresis curves of the Fe-FETs from one region to another.

interface, a top gate Al electrode was deposited by thermal evaporation with a shadow mask, as shown in Figure 1. Subsequent O_2 reactive ion etching (RIE) was done not only to allow for easy probe tip access of the bottom source/drain for measurement, but also for the reduction of gate leakage by effective cell-to-cell separation. Both cross-sectional and plane views of a fabricated Fe-FET are shown in the scanning electron microscope (SEM) and optical microscope (OM) images in Figure 1.

We employed a 4-inch-scale PDMS mold containing micropatterns with various shapes and dimensions, as schematically depicted in Figure 2a. SCEP using the PDMS mold on a blended TIPS-PEN:PαMS film allowed for fabrication of well-defined micropatterns on the film that were uniformly developed over the whole 4-inch wafer, as shown in Figure 2b. Examination of the micropatterns with OM in Figure 2c revealed details of the shapes and dimensions of the patterns. For instance, periodic hexagons, squares, and lines with sizes of 2, 5, 10, or 20 μm were easily printed. In addition, micrometer-scale letters and other geometric figures were readily obtained. Similar micropatterns were also obtained with diF-TES-ADT:PTAA blend films by SCEP.

It is also important to investigate the molecular and microscale structures of the patterned TIPS-PEN:PαMS blend film. As shown in Figure 2d, under cross-polarized OM, the patterned regions exhibited very strong optical birefringence, which arose from the anisotropic crystal growth of TIPS-PEN. The micro-texture shown in the optical micrograph image of Figure 2d arose from different crystal orientation of each domain characterized by birefringence TIPS-PEN crystals with different rotational angles with respect to crossed polarizers. To confirm the uniformity of our patterned TIPS-PEN/PαMS blend film, we examined surface profile of the film by AFM in height contrast. The films were very uniform in thickness with their rms roughness of approximately 1.5 nm (see the Supporting information, S1). The molecular structure of the patterned TIPS-PEN and PαMS blend thin film was further investigated using grazing-incidence X-ray Diffraction (GIXD), and the observation of spot-like multiple reflections clearly indicate that a single-crystalline TIPS-PEN texture was developed, even with the blend film, as shown in the inset of Figure 2d. The 2D GIXD pattern with an incident X-ray beam angle of approximately 0.15° from the film surface clearly exhibits three characteristic reflections on the "meridian" of the diffraction pattern corresponding to (00l) reflections of the TIPS-PEN crystals. Several off-meridian peaks corresponding to the group (0kl) reflections are also apparent.[45] The single crystalline nature of TIPS-PEN was not rarely altered during the patterning process in which structural defects may occur at the edges of individual micropatterns. No difference of 2D X-ray pattern with the

patterned film was observed from one with homogeneous, uniform blend film (see the Supporting information, S2).

The out-of-plane XRD diffraction pattern of the micropatterned TIPS-PEN:PαMS blend film shown in Figure 2e shows a set of (00l) reflections of the trigonal structure of TIPS-PEN crystals at room temperature (a = 0.775 nm, b = 0.773 nm, c = 1.676 nm, α = 89.5°, β = 78.7°, γ = 84°). A selected area electron diffraction (SAED) pattern of the TIPS-PEN, obtained using a transmission electron microscope (TEM), confirms that the c planes of TIPS-PEN are oriented parallel to the substrate with strong (020) and reflections, as shown in the inset of Figure 2e.[46] The strong tendency for commensurate growth with the strength of the intermolecular $\pi-\pi$ interactions allowed for the formation of laminated TIPS-PEN crystal. Both the in-plane and out-of-plane diffraction results clearly suggest that single crystal-like flat and homogeneous TIPS-PEN domains were well-formed, even in the blend film with PαMS, upon rapid spin-coating on the PVP layer. SCEP also produced various well-defined micropatterns using diF-TES-ADT:PTAA blend films with similar single-crystalline textures (see the Supporting information, S3).

The height profile of the patterned surface obtained by AFM shows a clear height difference between patterned and non-patterned regions of approximately 30 nm. In addition, the very smooth surface of the non-patterned regions is apparent (see the Supporting information, S4). Interestingly, these results indirectly suggest that the spin-coating of a blended solution on a PVP surface produced a uniform film in which thin and flat single-crystal-like TIPS-PEN layers were formed on top of the PαMS film on the PVP surface. Complete removal of TIPS-PEN molecules upon SCEP was confirmed by an experiment in which a thin blended film was treated in the same conditions as SCEP using a flat and uniform PDMS plate. No X-ray scattering reflections were obtained from the TIPS-PEN crystals (see the Supporting information, S5). This type of vertical phase separation of a polymer blend solution frequently occurs when there is a large difference in the solubility of the two components in a solvent.[47] In the current system, TIPS-PEN, which has poorer solubility, was the first phase separated at the blend solution/air interface, at which solution concentration was the highest because of solvent evaporation to the air phase. PαMS, which has better solubility in tetralin, was subsequently phase separated and solidified beneath the previously formed top layer. This ultrathin semiconducting layer vertically separated on an insulating polymer one is apparently beneficial for mechanically flexible memory devices as shown later.

The patterned blend semiconductor films were successfully utilized as channel layers in Fe-FETs, which allowed for well-defined channel dimensions as well as effective cell-to-cell separation. We employed periodic lines in a blended film bridged between source and drain electrodes, as schematically depicted in Figure 1a. The channel dimensions were precisely controlled by the number of microlines across the two electrodes. Two types of periodic lines, with widths of 50 and 20 μm, were micropatterned by SCEP on 18 pre-patterned sets of source and drain electrodes, followed by top gate deposition. A batch of 18 Fe-FET devices with either 20 or 50 μm periodic line channels of TIPS-PEN:PαMS blend films shows very reliable nonvolatile memory performance with well-saturated hysteresis of the source and drain current (I_{DS}) curve as a function of gate voltage (V_G), as representatively shown in Figure 3a.

The current between the source and drain increased sharply at a zero gate voltage and was saturated at a gate bias greater than −60 V due to the p-type characteristics of TIPS-PEN (see the Supporting information, S6). When the gate voltage decreased to zero, the I_{DS} remained at its saturated ON state of approximately 1×10^{-6}A, which arose from the nonvolatile remanent polarization of the ferroelectric PVDF-TrFE insulator. The subsequent positive gate bias on the device gradually switched polarization direction, giving rise to a rapid decrease in I_{DS}. The low current level, OFF state I_{DS} remained after the positive gate voltage was again removed due to the non-volatility of the polarization of PVDF-TrFE, as shown in Figure 3a. Both types of Fe-FETs, with 50 and 20 μm periodic line semiconducting channels, exhibited high ON/OFF current bistability of approximately 1×10^4, which was comparable with the value of the Fe-FET with a non-patterned, homogeneous blend film. This suggests that the semiconducting channels of the devices were not damaged during the patterning process or following the deposition of a ferroelectric polymer (see the Supporting information, S7). In general, devices with patterned blend films had slightly lower ON current levels as opposed to nonpatterned films because of the reduction in channel area. The effective cell-to-cell separation by patterned blend films also reduced the OFF current level relative to flat films, making the overall ON/OFF ratio of the patterned devices comparable with that of nonpatterned devices.

The statistical variations in the ON/OFF ratio values of the Fe-FETs containing micropatterned TIPS-PEN:PαMS blend films shown in Figure 3b suggest that our SCEP is suitable for fabrication of arrays of Fe-FETs. The patterning of the semiconducting channel layers reduced the cell-to-cell distribution of the ON/OFF ratio for both types of blend films. Furthermore, the devices with 50 μm periodic lines with both blend types displayed very narrow variation in the ON/OFF ratio. Since our technique relies on the thermal evaporation and diffusion of small semiconducting molecules into PDMS mold, there must be a limitation in pattern resolution and the resolution also depended on the shape of the micropatterns.[42] Micropatterns with defective 20 μm lines showed large variation in device performance for both blended semiconducting films, as shown in Figure 3b. In our previous work with solution-grown single crystals of TIPS-PEN,[42] we have observed that in the case of squares, a square with well-defined sharp edges was obtained down to dimensions of 5 × 5 μm^2, below which the edges became blunt. Arrays of circular TIPS-PEN microdomains were developed with diameters as low as 2 μm. We have also investigated the line pattern resolution of SCEP with a blend film and the results are shown in the Supporting Information, S8. Pattern edge became rough when a PDMS mold was used with 20 μm line width. Well-defined line patterns with reasonably uniform surface were also developed with a mold with 10 μm line width but the lines with patched TIPS-PEN crystalline domains were produced when a mold was employed with 5 μm line width.

The contact resistance between semiconducting channel and source or drain electrode should be taken into account, arising from the bottom insulating layer of a vertically separated blend film in contact with Au source and drain electrode. In fact, the field effect mobility of a FET with a TIPS-PEN/PαMS blend film (~0.11 cm^2/(V s)) was lower than that of a FET with single-crystal TIPS-PEN (~0.36 cm^2/(V s)),[42] although the blend film contained nearly single-crystalline TIPS-PEN layer vertically phase-separated with PαMS. It should, however, be

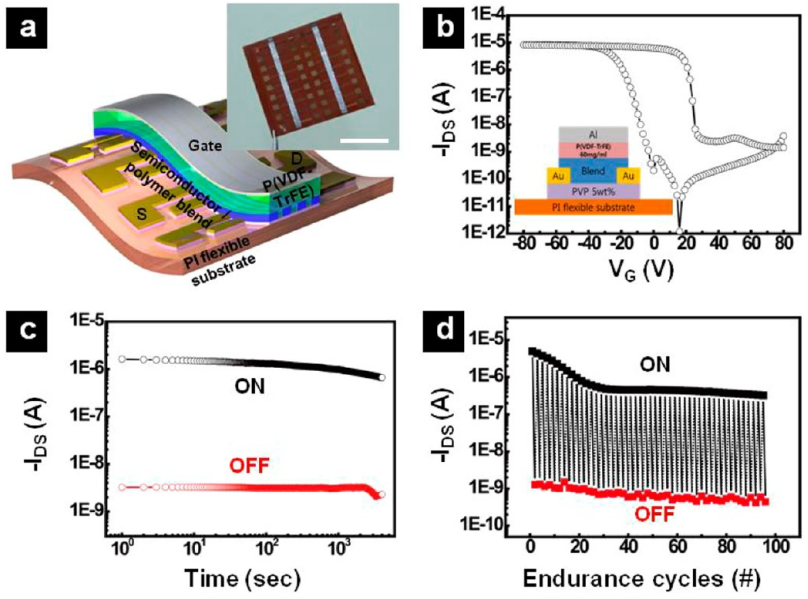

Figure 4. (a) Schematic of Fe-FET arrays with micropatterned semiconducting blend channels by SCEP on a flexible poly(imide) substrate. The arrays fabricated are shown in a photograph of the inset. (b) The I_{DS}-V_G transfer curve of a Fe-FET with 50 μm line-patterned TIPS-PEN:PαMS channel layer. The data retention (c, d) write/erase cycle endurance characteristics of flexible Fe-FET arrays with 50 μm patterned TIPS-PEN channels.

noted that the insulating PαMS film on Au source and drain electrode was much thinner than that in the channel regions due to the characteristic planarization phenomenon during spin coating of a blend solution. The ultrathin film formation over topography during spin-coating involves the competition of three major driving fields of surface tension, viscosity of a solution and shrinking speed. It is wel- known that the planarization of a film on a topographic surface renders the film on crest regions thinner than on trenches.[48] The planarization of ca. 50 nm thick blend film on a topology with 30 nm height in our case gave rise to approximately 20 nm thick film. The bottom insulating layer in particular on Au source and drain electrode was too thin to hinder the efficient carrier transport. As expected, when a blend film was thicker, the device performance became worse as characterized in the Supporting Information, S9.

The reliability of Fe-FETs with various patterned semiconducting channel layers was examined by data retention of both ON and OFF current state with time. We independently measured two nonvolatile I_{DS} values of Fe-FETs containing patterned TIPS-PEN:PαMS blend films set by different gate voltage sweeps at zero gate voltage with a constant V_{DS} of -5 V. Both the ON and OFF states of all devices examined were maintained longer than 1×10^4 seconds without any additional device encapsulation to protect the device from oxygen and water molecules, as shown in Figure 3c. Even continuous exposure of the devices to humidity of approximately 50% did not harm the device performance for a period longer than 80 days (see the Supporting Information, S10). Considering that most organic and polymeric semiconductors easily suffer under exposure to oxygen and water molecules, our patterned blend semiconducting layers are greatly beneficial when employed in a top gate architecture, because they can be additionally protected by the ferroelectric PVDF-TrFE channel layer and the top gate electrode. For multiple data write/erase endurance measurements, we consecutively read ON and OFF nonvolatile I_{DS} values with the programmed endurance cycle. Very consistent and reliable rewritable endurance was observed over 100 cycles, as shown in Figure 3d. Our device was still working even after more than 300 endurance cycles (data not shown). Similar results were also obtained for devices with diF-TES-ADT:PTAA blend films (see the Supporting Information, S11).

Wafer-scale arrays of Fe-FETs were produced by large-area SCEP for the patterned semiconducting layers in combination with monolithic film transfer of PVDF-TrFE, as shown in Figure 3e. In this fabrication process, the experimental conditions were further optimized for the complete wafer-to-wafer transfer of an approximately 700 nm thick PVDF-TrFE film spin-coated on a 4 in. wafer onto a patterned blended film on another 4 in. wafer. Exactly 162 Fe-FET devices were successfully fabricated with nine sets of arrays, each of which contained 18 cells, as shown in Figure 3e. All of the sets exhibited very uniform device performance with characteristic ferroelectric hysteresis curves. For instance, ON/OFF current bistability ratio values of approximately 10^4 did not vary much from one set to another, as shown in Figure 3f.

Our printing technique of blended semiconducting channel layers was also successfully applied to a polymeric substrate, for instance, polyimide (PI), on which arrays of high performance Fe-FETs with patterned semiconducting channels were successfully deposited, as schematically depicted in Figure 4a. The arrays of 18 Fe-FET devices on the PI substrate, as shown in the inset of Figure 4a, show uniform device performance and have potential for use as flexible memories. As shown, a ferroelectric I_{DS} hysteresis with an ON/OFF ratio of approximately 8×10^4 was well developed, which is very comparable with the value of Si substrate, as shown in Figure 4b. Again, high data reliability performance was observed and long-term data retention and repeated data write/erase cycle endurance were observed over 1×10^4 seconds and 100 cycle times, respectively, as shown in panels c and d in Figure 4.

Alternatively, arrays of Fe-FET devices with blend layers patterned on a PI substrate transiently attached on a glass

substrate with an adhesive layer were completely transferred to another substrate. Simple peel-off of the PI substrate with the device arrays from the glass substrate, followed by the transfer of the arrays onto a curved surface produced roll-up memory arrays, as shown in Figure 5a. The mechanically flexible PI

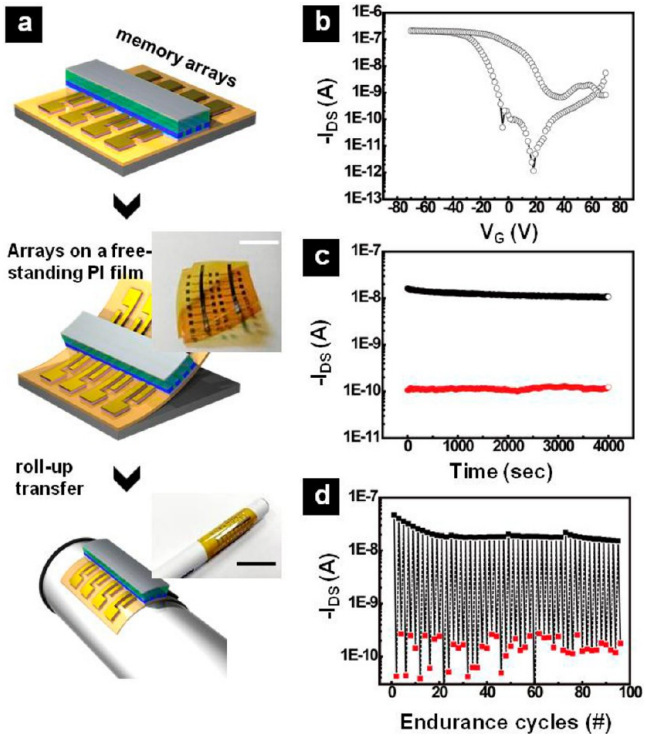

Figure 5. (a) Schematic illustration of roll-up memory arrays fabricated by detaching and transferring Fe-FET arrays on a flexible substrate with a transient adhesive layer onto the surface of a cylindrical ball-point pen. The insets in (a) show the photographs of the Fe-FET arrays at each fabrication step. The scale bars shown in the insets are 1 cm. (b) The $I_{DS}-V_G$ transfer curve of a Fe-FET mechanically deformed on the curved surface with 50 μm line patterned TIPS-PEN:PαMS channel layer. The data retention (c, d) write/erase cycle endurance characteristics of the deformed Fe-FET arrays with 50 μm patterned TIPS-PEN channels.

substrate with the Fe-FET arrays was in firm contact on the various non-planar substrates due to the adhesive layer. Again, the 18 Fe-FET devices on the curved substrate exhibit uniform device performance with high ON/OFF ratio of approximately 1×10^4, as shown in Figure 5b. High data reliability performance was also confirmed with long-term data retention and repeated data write/erase cycle endurance of 1×10^4 seconds and 100 cycle times, respectively, as shown in panels c and d in Figure 5. This transfer technique, which has already been developed for use with other electronic devices, was also successfully employed in nonvolatile ferroelectric memory devices in combination with our printing technique for micropatterning semiconducting blend channel layers. These versatile arrays of Fe-FETs have potential for use in many applications, such as high-definition electronic skins.

4. CONCLUSIONS

We demonstrated a wafer-scale large-area printing technique for micropatterning thin small-molecule semiconductor/polymer blend films suitable for arrays of nonvolatile top-gate/bottom-contact ferroelectric polymer FET memories. The selective contact evaporation printing (SCEP) of a blended film effectively removed low molecular weight semiconducting materials that were vertically phase segregated with an insulating polymer binder in regions of conformal contact with a PDMS mold, allowing for fabrication of a well-defined micropatterned semiconducting structure with a single crystalline texture. The arrays of Fe-FET devices all exhibited highly reliable nonvolatile memory characteristics with patterned semiconducting channels produced from two blends: TIPS-PEN:PαMS and diF-TES-ADT:PTAA. Specifically, they showed narrow performance variation with large ON/OFF current bistability ratios and good data retention over time. Furthermore, the scale-up of our SCEP allowed for the fabrication of arrays of 162 Fe-FET devices on a 4-inch Si wafer with patterned semiconducting channels in combination with a monolithic ferroelectric PVDF-TrFE film transfer technique. To demonstrate the versatility of our printing process, we not only developed arrays of high-performance Fe-FET devices on a flexible polymeric substrate but also roll-up memory arrays on a curved surface with detaching and transfer technique. The results suggest a novel design strategy for low-cost high-fidelity organic memory conveniently adoptable for various flexible organic electronic devices. Furthermore, our versatile micro-printing technique of blended semiconducting layers offers great potential in use of many other organic devices such as transistors and displays.

■ ASSOCIATED CONTENT

Supporting Information

Optical images, AFM, SEM images, GIXD data, and OFET and Fe-FET results. This material is available free of charge via the Internet at http://pubs.acs.org/.

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Notes

The authors declare no competing financial interest.

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